

Design Brief: 2027 Tesla BMS Hardware Sponsorship Application (Option A: ADI Package)

Team: Poliba Corse | **Vehicle Class:** Formula SAE Electric 2027 | **Target:** FSAE Italy / FS Germany

1. Accumulator Architecture & Operating Margins

The tractive system accumulator is organized as **140s 3p** (5 Ah cells, $I_{\text{cont}} = 60$ A) across 5 galvanic segments (**28s 3p** each). To maximize cell longevity and mitigate degradation across charging and discharging cycles, operating limits are clamped with conservative safety margins: $V_{\text{min}} = 2.67$ V (10% derating from absolute cutoff) and $V_{\text{max}} = 4.1$ V (5% margin below chemistry limit).

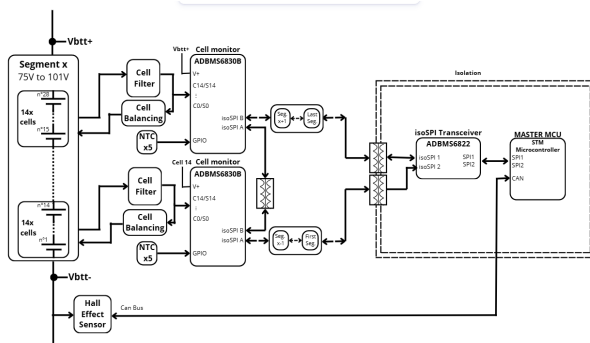
Parameter	Pack / Segment Design Value
Topology	140s 3p (5 Segments $\times$ 28s 3p)
Nominal Voltage (V_n)	504.0 V pack (100.8 V / segment)
Max Operating Voltage	574.0 V pack (114.8 V / segment)
Min Operating Voltage	373.8 V pack (74.76 V / segment)
Capacity & Rated I_n	15 Ah / 180 A continuous
DC Res. (SOC 50%)	0.597 Ω pack (0.119 Ω / segment)
Stored Energy	7.560 kWh (27.22 MJ) [1.512 kWh seg.]
Cell Mass	29.82 kg pack (5.964 kg / segment)

2. Sponsored Hardware Selection (ADI Package)

We selected the **ADI Package** to establish an automotive-grade, high-immunity daisy-chain network optimized for electric racing:

- **ADBMS6830B (AFE):** 16-channel multicell battery monitors deployed with 2 ICs per slave board (14 channels each). Synchronous dual $\Delta\Sigma$ converters (C-ADC and S-ADC) provide continuous redundant cell acquisition, passive balancing (up to 300 mA), and integrated diagnostic coverage for latent hardware faults.
- **ADBMS6822 (isoSPI Transceiver):** Dual isolated transceiver located on the TSAC Master Board. It bridges the differential isoSPI daisy-chain communication across all 5 segments directly to the host microcontroller via high-speed SPI.
- **High-Noise Immunity:** Reversible 2-wire isoSPI architecture eliminates complex intra-pack CAN networks and provides high RF/EMI immunity against inverter switching noise.

3. Distributed System Architecture & TSAC Integration



4. Monitoring, Diagnostics & FSAE Compliance

- **Single-PCB Segment Architecture:** Each 28s module houses 1 PCB integrating $2 \times$ ADBMS6830B (Bottom/Top) linked through 22 nF capacitors on-board. This eliminates intra-module high-voltage harnesses and avoids local microcontrollers inside cell bays.
- **Redundant ADC Comparison:** Dual-ADC architecture continually compares C-ADC and S-ADC conversions on every channel to flag conversion drift or analog front-end anomalies in real time.
- **Thermal Sensing Coverage:** NTC thermistors on cell tabs connect to the GPIO channels of each monitor IC, monitoring over 35% of total cells (exceeding the 30% regulatory requirement).
- **Open-Wire Integrity:** Built-in odd/even multiplexed open-wire diagnostic routines run periodically to verify balance lead connectivity.

5. Implementation & Validation Roadmap

- **Phase 1: Driver Bring-up on Evaluation Hardware:** Develop and validate SPI/isoSPI drivers on the target microcontroller utilizing the sponsored **EVAL-ADBMS6822-TSY** and ADBMS6830B demo boards. Confirm CRC/PEC execution and timing.
- **Phase 2: Segment PCB Prototyping:** Fabricate revision-1 28s slave boards; validate thermal dissipation during passive balancing and assess noise immunity under high inverter load conditions.
- **Phase 3: Hardware-in-the-Loop (HIL) Testing:** Execute automated fault-injection routines (overvoltage, undervoltage, sensor disconnects) to verify error detection latency and diagnostic logging.
- **Phase 4: Full Pack Integration & Track Testing:** Complete mechanical and electrical assembly inside the TSAC container; perform pack-level dyno validation and track testing for the 2027 season.